L Number	Hits	Search Text	DB	Time stamp
5	65968	(crosstalk or nois$4) same signal and magnitude	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:33
6	67768	first same inverter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:48
7	66822	second same inverter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:49
8	51186	(first same inverter) same (second same inverter)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:34
9	3060	((crosstalk or nois$4) same signal and magnitude) and ((first same inverter) same (second same inverter))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:34
10	926	(((crosstalk or nois$4) same signal and magnitude) and ((first same inverter) same (second same inverter))) and insert$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:35
11	847	((((crosstalk or nois$4) same signal and magnitude) and ((first same inverter) same (second same inverter))) and insert$5) and (ratio or size or larger or smaller)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:37
12	3	(((((crosstalk or nois$4) same signal and magnitude) and ((first same inverter) same (second same inverter))) and insert$5) and (ratio or size or larger or smaller)) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:40
13	3	((((((crosstalk or nois$4) same signal and magnitude) and ((first same inverter) same (second same inverter))) and insert$5) and (ratio or size or larger or smaller)) and 716/$.ccls.) and node	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:40
14	318	(((((crosstalk or nois$4) same signal and magnitude) and ((first same inverter) same (second same inverter))) and insert$5) and (ratio or size or larger or smaller)) and node	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:41
15	181	((((((crosstalk or nois$4) same signal and magnitude) and ((first same inverter) same (second same inverter))) and insert$5) and (ratio or size or larger or smaller)) and node) and CMOS	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:41
16	170	(((((((crosstalk or nois$4) same signal and magnitude) and ((first same inverter) same (second same inverter))) and insert$5) and (ratio or size or larger or smaller)) and node) and CMOS) and logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:42
17	29361	first near5 inverter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:48

18	30368	second near5 inverter	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:49
19	17576	(first near5 inverter) same (second near5 inverter)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:49
20	2533	((first near5 inverter) same (second near5 inverter)) and insert$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 07:01
21	236	(((first near5 inverter) same (second near5 inverter)) and insert$5) and ((crosstalk or nois$4) same signal and magnitude)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:50
22	115	((((first near5 inverter) same (second near5 inverter)) and insert$5) and ((crosstalk or nois$4) same signal and magnitude)) and node	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:50
23	72	(((((first near5 inverter) same (second near5 inverter)) and insert$5) and ((crosstalk or nois$4) same signal and magnitude)) and node) and CMOS	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:50
24	247	((first near5 inverter) same (second near5 inverter)) same insert$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:51
25	17	(((first near5 inverter) same (second near5 inverter)) same insert$5) and ((crosstalk or nois$4) same signal and magnitude)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:51
26	4665	((crosstalk or nois$4) same signal) and ((pair or two) near4 inverter)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:56
27	1675	(((crosstalk or nois$4) same signal) and ((pair or two) near4 inverter)) and magnitude	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:57
28	973	((((crosstalk or nois$4) same signal) and ((pair or two) near4 inverter)) and magnitude) and ratio	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:57
29	512	(((((crosstalk or nois$4) same signal) and ((pair or two) near4 inverter)) and magnitude) and ratio) and node	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:57
30	451	((((((crosstalk or nois$4) same signal) and ((pair or two) near4 inverter)) and magnitude) and ratio) and node) and series	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:58
31	7	(((((((crosstalk or nois$4) same signal) and ((pair or two) near4 inverter)) and magnitude) and ratio) and node) and series) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:59

32	1094	((first near5 inverter) same (second near5 inverter)) same (ratio or size or larger or smaller)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 07:02
33	75	(((first near5 inverter) same (second near5 inverter)) same (ratio or size or larger or smaller)) and ((crosstalk or nois$4) same signal and magnitude)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 07:02
-	306886	(crosstalk or nois$4) same signal	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/17 06:55
-	37051	insert$5 same (buffer or inverter)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/15 17:08
-	347	((crosstalk or nois$4) same signal) same (insert$5 same (buffer or inverter))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/15 17:10
-	14	((((crosstalk or nois$4) same signal) same (insert$5 same (buffer or inverter))) and logic) and 716/$.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/15 17:19
-	169	(((crosstalk or nois$4) same signal) same (insert$5 same (buffer or inverter))) and logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/11/15 17:27

	Document ID	Issue Date	Pages	Title	Current OR
1	US 20030159121 A1	20030821	8	Variable stage ratio buffer insertion for noise optimization in a logic network	716/8
2	US 20030123279 A1	20030703	10	Silicon-on-insulator SRAM cells with increased stability and yield	365/154
3	US 20030117301 A1	20030626	46	Methods, apparatus, and systems for reducing interference on nearby conductors	341/55
4	US 20030117184 A1	20030626	49	Methods, apparatus, and systems for reducing interference on nearby conductors	327/94
5	US 20030117183 A1	20030626	47	Methods, apparatus, and systems for reducing interference on nearby conductors	327/94
6	US 20030116827 A1	20030626	46	Methods, apparatus, and systems for reducing interference on nearby conductors	257/650
7	US 20020080883 A1	20020627	213	Signal transmission system for transmitting signals between LSI chips, receiver circuit for use in the signal transmission system, and semiconductor memory device applying the signal transmission system	375/257
8	US 20010035548 A1	20011101	114	Dynamic random access memory	257/296
9	US 6646970 B1	20031111	13	Thermomagnetic writing of pulse sequences of controlled magnitude and variably controlled duration	369/59.11
10	US 6583629 B1	20030624	21	Magnetic digital signal coupler monitor	324/632
11	US 6580411 B1	20030617	72	Latch circuit, shift register circuit and image display device operated with a low consumption of power	345/98

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12	US 6493394 B2	20021210	209	SIGNAL TRANSMISSION SYSTEM FOR TRANSMITTING SIGNALS BETWEEN LSI CHIPS, RECEIVER CIRCUIT FOR USE IN THE SIGNAL TRANSMISSION SYSTEM, AND SEMICONDUCTOR MEMORY DEVICE APPLYING THE SIGNAL TRANSMISSION SYSTEM	375/257
13	US 6492847 B1	20021210	8	Digital driver circuit	327/112
14	US 6413830 B1	20020702	111	Dynamic random access memory	438/386
15	US 6410379 B1	20020625	111	Method of forming a submerged semiconductor structure	438/222
16	US 6377638 B1	20020423	208	SIGNAL TRANSMISSION SYSTEM FOR TRANSMITTING SIGNALS BETWEEN LSI CHIPS, RECEIVER CIRCUIT FOR USE IN THE SIGNAL TRANSMISSION SYSTEM, AND SEMICONDUCTOR MEMORY DEVICE APPLYING THE SIGNAL TRANSMISSION SYSTEM	375/348
17	US 6335896 B1	20020101	113	Dynamic random access memory	365/230.03
18	US 6157688 A	20001205	211	Signal transmission system for transmitting signals between LSI chips, receiver circuit for use in the signal transmission system, and semiconductor memory device applying the signal transmission system	375/348

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19	US 6118318 A	20000912	11	Self biased differential amplifier with hysteresis	327/206
20	US 6088246 A	20000711	25	Method of and device for controlling pulse width modulation inverter	363/41
21	US 6087901 A	20000711	39	Tuning amplifier	330/305
22	US 6043810 A	20000328	39	Digitizer controller	345/173
23	US 6028798 A	20000222	18	Low voltage test mode operation enable scheme with hardware safeguard	365/201
24	US 6002618 A	19991214	40	NMOS input receiver circuit	365/189.05
25	US 5986463 A	19991116	24	Differential signal generating circuit having current spike suppressing circuit	326/27
26	US 5973533 A	19991026	42	Semiconductor gate circuit having reduced dependency of input/output characteristics on power supply voltage	327/263
27	US 5959480 A	19990928	16	Digital signal transition edge alignment using interacting inverter chains	327/161
28	US 5950145 A	19990907	18	Low voltage test mode operation enable scheme with hardware safeguard	702/109
29	US 5870346 A	19990209	40	VLSI memory circuit	365/226
30	US 5825700 A	19981020	18	Low voltage test mode operation enable scheme with hardware safeguard	365/201

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31	US 5812079 A	19980922	27	Subranging type A/D converter apparatus equipped with feedback line for transmitting control signal for A/D conversion	341/163
32	US 5796671 A	19980818	112	Dynamic random access memory	365/230.03
33	US 5793775 A	19980811	20	Low voltage test mode operation enable scheme with hardware safeguard	714/724
34	US 5771163 A	19980623	13	AC-DC converter apparatus	363/71
35	US 5764110 A	19980609	32	Voltage controlled ring oscillator stabilized against supply voltage fluctuations	331/57
36	US 5708386 A	19980113	17	CMOS output buffer with reduced L-DI/DT noise	327/380
37	US 5632019 A	19970520	19	Output buffer with digitally controlled power handling characteristics	713/300
38	US 5617062 A	19970401	51	Timing circuit with rapid initialization on power-up	331/111
39	US 5608687 A	19970304	41	Output driver control for ROM and RAM devices	365/233.5
40	US 5594361 A	19970114	23	Logic gate with controllable hysteresis and high frequency voltage controlled oscillator	326/24
41	US 5521556 A	19960528	26	Frequency converter utilizing a feedback control loop	331/1R
42	US 5491441 A	19960213	6	Method and apparatus for generating a clock signal from a continuous oscillator signal including a translator circuit	327/291

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43	US 5487038 A	19960123	41	Method for read cycle interrupts in a dynamic read-only memory	365/191
44	US 5459437 A	19951017	25	Logic gate with controllable hysteresis and high frequency voltage controlled oscillator	331/111
45	US 5444410 A	19950822	17	Controlled-transitioni-time line driver	327/317
46	US 5408235 A	19950418	43	Second order Sigma-Delta based analog to digital converter having superior analog components and having a programmable comb filter coupled to the digital signal processor	341/143
47	US 5262686 A	19931116	11	Differential chopper type comparator	327/77
48	US 5063490 A	19911105	54	Regulated chopper and inverter with shared switches	363/37
49	US 5021785 A	19910604	9	Floating point digital to analog converter with bias to establish range midpoint	341/138
50	US 5012142 A	19910430	11	Differential controlled delay elements and skew correcting detector for delay-locked loops and the like	327/281
51	US 5001367 A	19910319	13	High speed complementary field effect transistor logic circuits	326/108
52	US 4890022 A	19891226	13	Delay circuit device utilizing the Miller effect	327/261

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53	US 4868422 A	19890919	7	TTL compatible CMOS logic circuit for driving heavy capacitive loads at high speed	326/71
54	US 4820937 A	19890411	11	TTL/CMOS compatible input buffer	326/71
55	US 4796227 A	19890103	34	Computer memory system	365/154
56	US 4672243 A	19870609	8	Zero standby current TTL to CMOS input buffer	326/71
57	US 4665327 A	19870512	7	Current to voltage interface	326/64
58	US 4486703 A	19841204	15	Boost voltage generator	323/222
59	US 4479161 A	19841023	16	Switching type driver circuit for fuel injector	361/154
60	US 4441165 A	19840403	51	Real-time ordinal-value filters utilizing complete intra-data comparisons	708/207
61	US 4368354 A	19830111	18	Discriminator apparatus for detecting the presence of a signal by using a differential beat signal having an inaudible frequency	348/485
62	US 4352000 A	19820928	22	Induction heating cooking apparatus	219/626
63	US 4285319 A	19810825	17	Air flow amount adjusting system for an internal combustion engine	123/682
64	US 4256974 A	19810317	7	Metal oxide semiconductor (MOS) input circuit with hysteresis	326/70
65	US 4192268 A	19800311	17	Air flow amount adjusting system for an internal combustion engine	123/700
66	US 4187854 A	19800212	16	Implantable demand pacemaker and monitor	607/33

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67	US 4172459 A	19791030	16	Cardiac monitoring apparatus and monitor	600/510
68	US 4166470 A	19790904	15	Externally controlled and powered cardiac stimulating apparatus	607/33
69	US 4114055 A	19780912	8	Unbalanced sense circuit	327/57
70	US 4083008 A	19780404	14	Method and circuit for generation of digitally frequency-shiftable electric signals	375/303
71	US 4004170 A	19770118	5	MOSFET latching driver	327/209
72	US 3983543 A	19760928	16	Random access memory read/write buffer circuits incorporating complementary field effect transistors	365/205
73	US 3825691 A	19740723	19	F-T RADA RECEIVER WITH LEVEL DISCRIMINATION	370/436
74	US 3708688 A	19730102	10	CIRCUIT FOR ELIMINATING SPURIOUS OUTPUTS DUE TO INTERELECTRODE CAPACITANCE IN DRIVER IGFET CIRCUITS	326/28
75	US 3575085 A	19710413	55	ADVANCED FIRE CONTROL SYSTEM	235/404